Abstract of the Disclosure

An encryption device of the present invention eliminates data contention and minimizes area by using a faster memory that can access data multiple times within a given time. An encryption device for performing encryption of plain text blocks using data encryption standard algorithm, wherein the encryption device includes an initial permutation unit, a data encryption unit having n-stage (n is an even number equal to or larger than four) pipeline structure using a first clock and a second clock and an inverse initial permutation unit, the encryption device comprising: a multiplexer for selecting one of a half of n 48-bit inputs; 8 S-Boxes, each for receiving 6-bit address among the selected 48-bit and outputting 4-bit data; a demultiplexer for distributing 4-bit data from each of the S-Boxes to the half of n outputs; and a controller for control the multiplexer and the demultiplexer with a third clock and a fourth clock, wherein the third and the fourth clock are faster than the first and the second clocks by n/2 times.